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<u>L19</u>	L18 and operating system and (address\$ near4 (translat\$ or transform\$ or map\$))	1	<u>L19</u>
<u>L18</u>	(modif\$ or chang\$ or alter) near5 content near5 (active or real\$ Or machne\$) and guest\$	9	<u>L18</u>
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<u>L16</u>	4456954.pn.	1	<u>L16</u>

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<u>L14</u>	(modif\$ Or chang\$ or alter) near5 content\$ near5 guest\$ near4 (active\$ or real\$) and cache and (tlb or buffer)	0	<u>L14</u>
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<u>L12</u>	L11 and (creat\$ or generat\$ or develop\$ Or mak\$)	1	<u>L12</u>
<u>L11</u>	l6 and data near4 (structure\$ or process\$)	1	<u>L11</u>
<u>L10</u>	l1 and (modif\$ or chang\$ Or alter) near5 data structure\$	1	<u>L10</u>
<u>L9</u>	6075938.pn.	1	<u>L9</u>
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<u>L6</u>	5381535.pn.	1	<u>L6</u>
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<u>L4</u>	L1 and (active\$ near4 translat\$) and (operating system) and (guest near4 operating)	2	<u>L4</u>
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<u>L2</u>	L1 and (active\$ near4 translat\$)	3	<u>L2</u>
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1 [Disco: running commodity operating systems on scalable multiprocessors](#)

Edouard Bugnion, Scott Devine, Kinshuk Govil, Mendel Rosenblum

 November 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 4

 Full text available: [pdf\(400.76 KB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

In this article we examine the problem of extending modern operating systems to run efficiently on large-scale shared-memory multiprocessors without a large implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine monitors. We use virtual machines to run multiple commodity operating systems on a scalable multiprocessor. This solution addresses many of the challenges facing the system software for these machines. We demonstrate our approach with a prototy ...

Keywords: scalable multiprocessors, virtual machines

2 [Architectural support for translation table management in large address space machines](#)

Jerry Huck, Jim Hays

 May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture**, Volume 21 Issue 2

 Full text available: [pdf\(1.34 MB\)](#)

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Virtual memory page translation tables provide mappings from virtual to physical addresses. When the hardware controlled Translation Lookaside Buffers (TLBs) do not contain a translation, these tables provide the translation. Approaches to the structure and management of these tables vary from full hardware implementations to complete software based algorithms. The size of the virtual address space used by processes is rapidly growing beyond 32 bits of address. As the utilized ad ...

3 [Architecture of the IBM system/370](#)

Richard P. Case, Andris Padegs

 January 1978 **Communications of the ACM**, Volume 21 Issue 1

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